REMARKS

Status of the Claims

In the Office Action, claims 1-28 were noted as pending in the application. All claims stand rejected.

A. Rejection of Claims 11-15, 17, 20-24 and 26 under 35 U.S.C. § 103(a).

On page 7 of the Office Action, claims 11-15, 17, 20-24 and 26 were rejected under 35 U.S.C. § 103 as being obvious over U.S. Patent Application Number US 2002/0088003 to Salee, ("Salee") in view of U.S. Patent Number 6,698,022 to Wu ("Wu"). The reasons that the claims patentably distinguish over the reference are addressed below.

B. Summary of Cited References

Before addressing the Examiner's rejections, a brief summary of the cited references is provided.

Salee

Salee relates to a system for providing redundancy in a data over cable network that includes a plurality of CMTSs. ¶ 2. A timer preset register in a master CMTS stores a preset value and a comparator initiates a SyncPulse signal to slave CMTSs when a timer value equals the value stored in the present register. ¶ 13. The timer preset value in every CMTS – including the master and all slaves - is set to the same value. ¶ 14 When the comparator of the master CMTS indicates a match between the preset register and the timer counter of the master, the SyncPulse signal then goes out to the slave CMTSs and instructs each salve to load the value from its respective preset register into its timer counter. *Id.*, ¶ 15, Claim 3. Thus, the timer counters of all CMTSs are synchronized at a frequency that is based on the value in the preset registers. ¶ 15. Changing the preset value P changes the time between SyncPulses being sent from the master to slave CMTSs. *Id.*

Wu

Wu relates to "recovering a global timing reference from a plurality of timestamps periodically transmitted from [a] CMTS." Col. 3, lines 60-62. To avoid using a relatively costly VCO, adjusts the local clock counter of a cable modem instead of adjusting the counter frequency. Col. 4, lines 48-50. To correct for jitter, clock drift and cable delays, a software interrupt is used to adjust the local timer clock value according to a mathematical algorithm that computes adjustment values based on timestamps received from a CMTS. Col. 6, lines 39-44. Thus, if modeling parameters are chosen correctly, the mathematical equation/algorithm can use received timestamp values and local clock values to estimate a jitter-free timestamp value T_c for every local clock counter t. Col. 5, lines 52-53.

C. The Claims are not Obvious over the Cited References

Applicant respectfully submits that the subject matter of the claims patentably distinguish over the cited references. Under MPEP § 2142, for an examiner to establish a *prima facie* case of obviousness, "three basic criteria must be met. First, there must be

some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure." If any of these three criteria are not met, the Examiner has not met the burden of establishing a *prima facie* case of obviousness, and the rejection should be withdrawn.

Furthermore, each dependent claim includes all of the limitations of the independent claim from which it depends. If an independent claim is non-obvious under 35 U.S.C. § 103, then any claim depending therefrom is non-obvious. MPEP §2143.03, citing In re Fine, 837 F.2d 1071 (Fed. Cir. 1988). Applicant respectfully submits that the burden of establishing a *prima facie* case of obviousness has not been met.

D. Claims are not obvious over the cited references

Regarding independent claims 11 and 20, a first value of a timing counter of a first circuit card is copied to a storage device, an offset is added to this value to create a future timing value that is then copied into the timing counter of a second circuit card. Claims 15 and 24 claim system hardware for facilitating the methods of claim 11 and 20. A timing value is written periodically from a system controller master to a circuit card slave. Page 14, lines 9-12. To obviate error caused by delay in writing the timing value from the master to the slave, a predetermined offset is added to the value of the master timing value before it is stored to the timing counter of the spare card. Page 14, lines 19-21. "The increased count value should be created such that the actual loading of this increased count value into the slave timing counters (after distribution from the system Controller card to the cable interface cards) will occur exactly when the master timing counter on the system Controller card arrives at the value which is equal to the increased value." Page 15, lines 7-11. This provides the advantage that when a spare circuit card takes over for a failed circuit card, the timestamps are sent out from the newly-placed-into-service spare card in continuity with the timestamp stream that had been provided by the previous circuit card that the spare replaced. Page 15, lines 11-12.

This procedure is helpful when, for example, a circuit fails and a spare is automatically swapped into service as a replacement for the failed card. Or, when a card is physically replaced with a new card, and the new card takes over for a currently active card - a previously spare card, for example. In the latter case, the new card might have an empty timing counter register - capable of storing a timing value - because it has been out of service (i.e., on a shelf in a warehouse, for example), and would thus need a value placed into its timing counter. When a current timing counter value is distributed from the System Controller, by the time the value reaches the slave circuit cards, a finite amount of time will have passed, and the value will be stale, inasmuch as it represents a time that is not contemporaneous with the actual current time of the System Controller. By determining the amount of delay that occurs in distributing the timing value from the System Controller to the individual circuit cards, compensation is provided by adding this delay amount to the timing value from the System Controller, and then writing the sum to a given circuit card. Then, timestamps transmitted to the newly-placed-into-service card

are time-continuous with the stream of timestamps that the previous card, which it replaces, had been transmitting.

This is distinguished from Salee in that the timing value in Salee is merely a predetermined value, representing a point in time, that occurs once every seven-minute (approximately) cycle. Par. 15. This value in Salee is an arbitrarily selected digital number placed into a register. Par. 13. This number is chosen to be a point in time from the set of points in time that will occur during a typical timing cycle, which the Salee applications states is approximately seven minutes. Thus, the arbitrary time P in Salee does not correspond to any jitter amount, delay amount, or time difference in bringing another device into service to replace a similar one that is taken out of service. It, the arbitrary time value P, is merely one of the plurality of incrementing time values that occur during a cycle, before the counters reset when another cycle begins. Basically, Salee teaches that active cards should be synchronized with one another at least once every timing cycle. This is also referred to in the first clause of the sentence of the present application that begins at page 13, lines 13-14, before the introduction of the claimed subject matter begins at page 13, line 16.

In contrast, the future timing counter value in the present application is a combination of the current timing value of the master timing controller value and an offset value. The offset value is chosen to equal the amount of time required to determine that a timing value needs to be inserted into a new card, and to actually update the new card's counter with the combined timing value. Thus, when the new card begins operating with the value that is transferred into it's timer, the same will be synchronized with the master system timing counter, which will have already advanced with respect to what it was when the determination was made that the new card needs to be pressed into service. Page 14, line 16 – page 15, line 12. Accordingly, the timing value P in Salee is not the same as the future timing value as described and claimed in the present application.

With respect to Wu, Examiner asserts that an offset is added to a timestamp, and that this is the same as adding a predetermined offset to a counter value to obtain a future timing value. Applicant disagrees. An offset is not added to a time stamp in Wu. Rather, an adjustment value is used to cause a change in a counter at a cable modem. Moreover, one of the adjustment values, C1, is not even added to the timestamp being operated on in Wu. In Wu, an adjustment is made to the second local clock counter based on C1, but C1 is not added to the timestamp in the second local clock counter. Rather, if C1 is a positive number, the second local clock counter is incremented by one. If C1 is a negative number, the second local clock counter is decremented by one. Col. 7, lines 30-34. Thus, adjusting the timestamp in the second local clock counter is not analogous to adding the claimed predetermined offset to the first timing value to obtain a future timing value.

Furthermore, the only value in the second local clock counter is the first time stamp that is received from the CMTS at the beginning of a given cycle, a new one of which begins with each interrupt. Col. 6, lines 50-52. Thus, C1 is not added to each timestamp value as the predetermined offset is in the present application. Moreover, a corrected timestamp is purported to be calculated in Wu according to equation (11). However, Wu does not disclose an equation (11). Therefore, it is indeterminate how the corrected timestamp advancement value is calculated.

Furthermore, this value is used in equation 13 to calculate the second local clock counter advancement value, which is in turn used to calculate C2 in equation 14. C2 is used to correct the second local counter each time a corrected timestamp is generated using C1 at step 740. Col. 7, line 41 – col. 8, line 4. "In the preferred embodiment [of Wu], the cable modem's MAC continually adjusts the second local clock counter by both the first and second adjustment values C1 and C2, respectively. Together, with the assistance of the ranging offset, these adjustments accurately synchronize the second local clock counter to the CMTS master clock counter." Col. 8, lines 5-11. In summary, Wu discloses using estimated values calculated according to a series of equations, one of which is not disclosed in the Wu specification, to adjust the local clock of a cable modem so that it is synchronized with the master clock of the CMTS. Applicant submits that the claims of the present invention do not read on Wu because it does not disclose adding a predetermined offset to a current timing value at the CMTS to arrive at a future timing value, that is then used to start the local timer of a newly-placed-into service cable interface card that is also at the CMTS.

Indeed, following adjustment, an adjusted value in Wu may not even be greater than its corresponding unadjusted value because in some instances the counters are decremented if C1 and/or C2 are negative. Col. 7, lines 30-32 & 66-67. Thus, the basis for the rejection originally made in the previous office action, as well as the reiteration of same in the current office action, is traversed. According to Examiner in the present office action, "[t]he interpretation of a 'future timing counter value' as any number that is greater in value that the output of a regularly-incrementing counter device is a reasonable interpretation of the claim language." Thus, consistent with Examiner's statement, a timing value that is reached by decrementing a counter cannot be a future timing value. It cannot be logical, therefore, for one skilled in the art to look at Wu, either standing alone, or in combination with Salee, to arrive at the invention as a whole as claimed in the claims, because all of the elements claimed in the independent claims are not found in the references, either individually or in combination with one another.

Notwithstanding that all of the elements of the claims are not found in the references, Examiner must demonstrate that a suggestion or teaching to combine the references exists. Since the concept of adding a predetermined offset to the current timing value of a counter to arrive at a future timing value is not found in the references, synthesizing such a motivation from passages within them is difficult. First, the claimed invention is generally applied to components that are located at the CMTS, which is located at a service provider's head end. Wu is concerned with adjusting the clock at a cable modem Also, Wu is concerned with periodically synchronizing cable modems with the CMTS clock, as the various modem clocks can drift apart due to changes in network temperature and impedance among other factors between the CMTS and the remotely located cable modems. Thus, Wu is concerned with addressing drift that naturally occurs in continuously variable amounts. The direction of drift can even be in the negative direction, and thus may require that a counter be decremented rather than incremented as discussed above.

In contrast, the present invention is directed toward compensating for the delay in loading a timing counter value from a master clock into the slave clock of a newly-placed-into-service device. This delay is typically always the same, as it depends on time required for writing and reading digital registers, which should generally always be the

same the same, assuming that the overall clock frequency is constant. Thus, there is no suggestion or motivation found in the references to combine Wu with Salee because neither Salee nor Wu discuss a future timing value as defined in the specification of the present application. Furthermore, the adjustment described in Wu is made to account for constantly changing factors that affect propagation delay in a network as opposed to the determinable delay in transferring a timing counter value from one device to another.

Notwithstanding that neither Wu nor Salee disclose a future timing value as defined in the present application, it appears that Examiner may have inadvertently used prohibited hindsight in attempting to piece together the claim limitations from the references. For example, Examiner stated in the present office action that even if Wu does not disclose calculating a future timing value as disclosed in the present application, "the alleged deficiency would not prohibit Wu from disclosing copying a first timing value into a storage device and adding an offset to create a future timing counter value." Page 4, lines 4-7. Examiner appears to be stating that even though a future timing value may not be found in Wu, Wu nevertheless discloses the copying and adding steps of claim 11. Applicant asserts that if Wu does not disclose use of a future timing value as defined in the present application, these other steps cannot be found in Wu either because the steps of copying and adding refer to operations performed on the defined future timing value. Thus, it appears that Examiner is attempting to apply generic process steps found in Wu to the present claims without showing a motivation to do so. Accordingly, it appears that hindsight was applied by using Applicant's claim limitations as a blueprint for combining elements from the references to arrive at the claimed invention. This is impermissible. In re Fritch, 972 F.2d 1260, 1266 (Fed.Cir. 1992).

Lastly, Examiner must show a likelihood of success in combining the references. If one assumes for purposes of argument that the references disclose the claimed limitations and that a suggestion or motivation for combing the references is demonstrated, a likelihood of success in combing the references must still be shown. As discussed above, for example, the adjustment values C1 and C2 of Wu may cause the adjustment to the relevant counter to be decremented instead of incremented. Thus, these adjustment values cannot be analogous to the future timing value used in the present application, because to use them as such would exacerbate, rather than cancel out, the effect of the delay in writing the timing counter value of the first cable interface circuit to the second. The claimed adding of the offset in claim 11 of the present application cancels the effect of transferring a timing value from the master clock to a new cable interface circuit. Thus, there cannot be a likelihood of success in combining the reference to arrive at the claimed limitation found in the independent claims. Accordingly, withdrawal of the rejection of claims 11, 15, 20 and 24 is respectfully requested.

Furthermore, since these claims are independent claims, all of the dependent claims that depend respectively therefrom are also not obvious. Therefore, withdrawal of the rejection of claims 12-14, 16-19, 21-23 and 25-28 is also respectfully requested under MPEP §§2142 §2143.03, as these dependent claims also patentably distinguish over the references.

SUMMARY

For all the reasons advanced above, Applicant respectfully submits that the application is in condition for allowance and that action is earnestly solicited.

If the Examiner believes that there are any issues that can be resolved by a telephone conference, or that there are any informalities that can be corrected by an Examiner's amendment please contact the undersigned at the mailing address, telephone, facsimile number, or e-mail address indicated below.

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Respectfully submitted,

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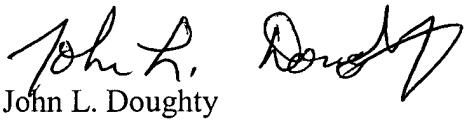

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